DERWENT-ACC-NO: 2001-577215
DERWENT-WEEK: 200165

TITLE: Stacked chip package

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
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APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001036630A	N/A	1999KR-0043732	October 11, 1999

INT-CL_(IPC): H01L023/28

ABSTRACTED-PUB-NO: KR2001036630A

BASIC-ABSTRACT: NOVELTY - A stacked chip package is provided to attain an increase in a data storage capacity and further to realize a mounting of high density.

DETAILED DESCRIPTION - The stacked chip package(100) includes lower and upper chips(30,40) attached to leads(20) and encapsulated in a package body(70). Each chip(30,40) has electrode pads(32,42) formed on an active surface thereof. The leads(20) are interposed between both chips(30,40) and attached to the active surface of the lower chip(30) by a double-sided adhesive tape(62) and the back surface of the upper chip(40) by an insulating

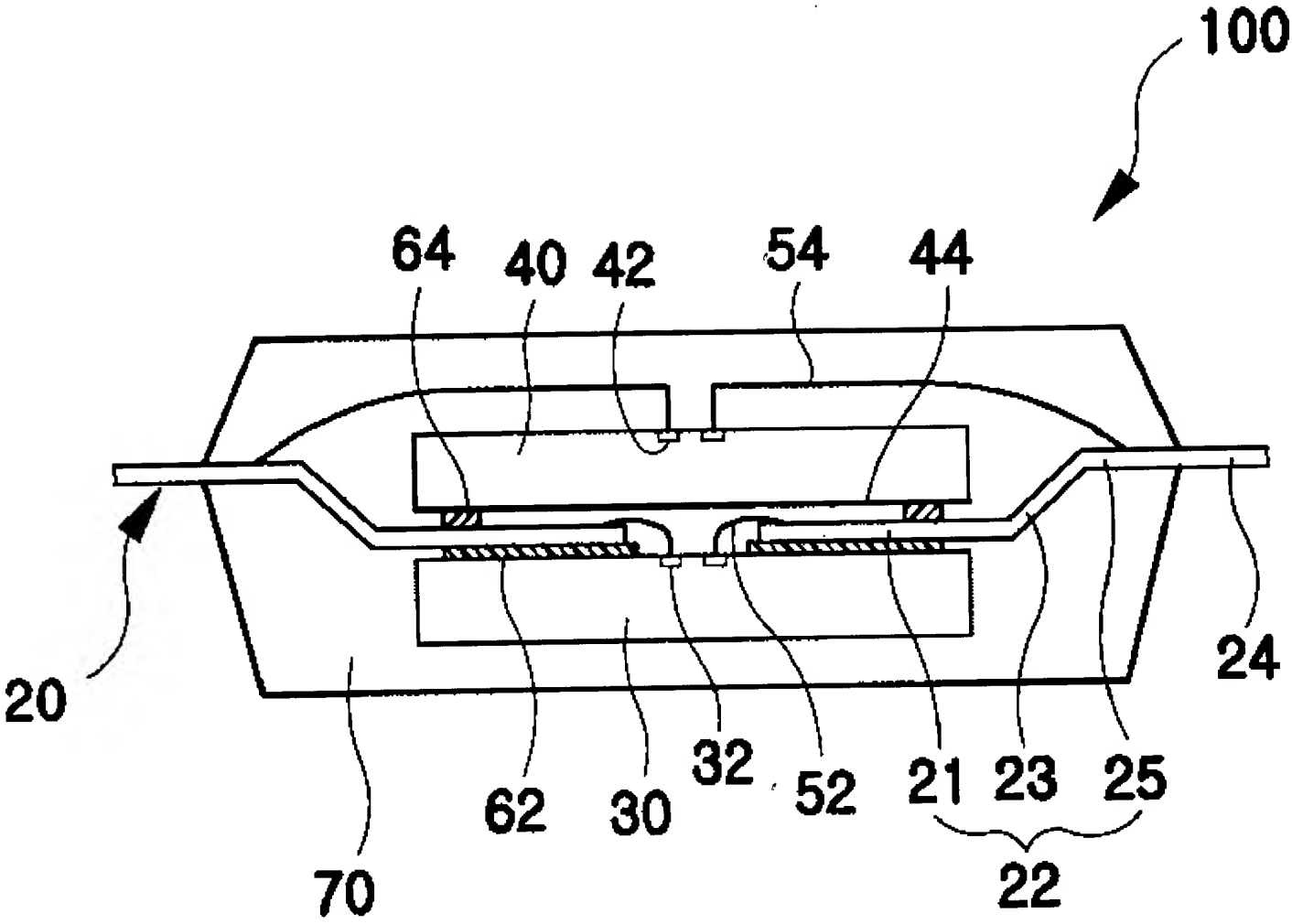
layer(64). In particular, the electrode pads(32) of the lower chip(30) are electrically connected to inner end portions of the corresponding leads(20) by lower metal wires(52), whereas the electrode pads(42) of the upper chip(40) are electrically connected to outer peripheral portions of the corresponding leads(20) by upper metal wires(54). Therefore, regardless of a size or a function, two chips(30,40) can be stacked together in the single package body(70).

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS:
STACK CHIP PACKAGE

DERWENT-CLASS: U11

EPI-CODES: U11-E02A1;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